Generation of High-Speed Pseudorandom Sequences Using Multiplex-Techniques

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***Abstract*—We report on the design and performance of high-speed pseudorandom sequence generators for nonreturn-to-zero (NRZ)-signals. The hardware is based on multiplexer circuits that multiply the data rate of a 5 Gb/s pseudorandom sequence to, respectively, 10 and 20 Gb/s. We employ multiplex-techniques based on the "cycle-and-add property" of pseudorandom sequences. The circuitry incorporates special high-speed silicon chips and is fabricated in both microstrip and coplanar waveguide technology. The experimental results demonstrate the feasibility of our approach.**

I. Introduction

IN RECENT years, the demand for optical transmission systems has been increasing rapidly and there exist significant efforts to improve the transmission capacities. In general, higher bit rates can be achieved both by improving the bit rate of single-channel systems, which multiplex the signal in the time domain (TDM-systems) as well as by using multichannel systems, which multiplex the signals in the wavelength domain and therefore multiply the bit rate of each channel by the number of channels (WDM-systems) [1]. The total bit rate attainable with a combination of TDM and WDM is expected to be in the Tb/s range [2]. Since there are several possibilities to overcome the dispersion problems which prevent a further increase of the bit rate of TDM-systems [1], and since the respective electronic components can be provided [3], it seems possible to realize TDM-systems operating with data rates of 40 Gb/s or more within the next years.

The present work arose from a requirement of high-speed pattern generation for the development of an optical 20 Gb/s data transmission system (Fig. 1). A device under test (DUT) is experimentally tested by the use of a pseudorandom sequence as a test string. Fast pseudorandom sequences can be obtained by multiplying the data rates of sequences which are derived from low-speed pulse pattern generators using special multiplex-techniques [4], [5] and considering the "cycle-and-add-property" [6]. For a reasonable hardware implementation it is important that long delay times are avoided by the use of EXOR operations in order to maintain the maximum word length at the output of the multiplying stages.

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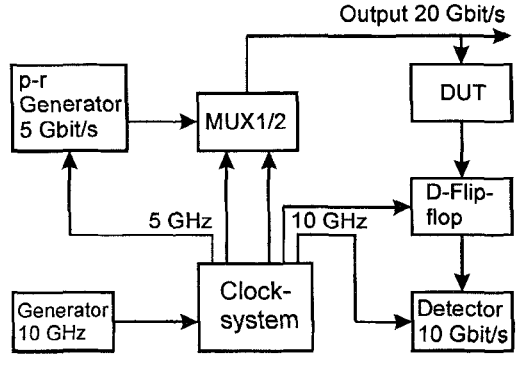

Fig. 1. Application of the pseudorandom generator.

In Section II, the multiplex-technique is described and applied to a standardized sequence [7] using a length of $L = 2^{23} - 1$ b. Based on the multiplex-technique and applying the high-speed chips described in Section III, Section IV introduces a circuit which generates a 10 Gb/s pseudorandom sequence. Then, the generation of a 20 Gb/s sequence utilizing coplanar waveguide technology is described yielding finally a 20 Gb/s pseudorandom sequence.

II. Operational Principle

By splitting a pseudorandom sequence into even and odd clock cycles, one gets two new identical sequences with a different phase and the data rate divided by two [4], [5]. Inverting this procedure and combining two identical but phase-shifted sequences in a multiplexer the data rate of the sequence is doubled. By an analogeous procedure we can multiply the data rate by $4, 8, \cdots, 2n-1$, with n being the number of shift register stages which produce the pseudorandom sequence. The length of the sequence is derived from n as $L = 2^n - 1$. Since in the following we are interested in multiplying the data rate by two, we will treat only the first case. If we asume the multiplexing of two identical sequences $\{a_k\}$ and $\{b_k\}$, the element a_k has to be followed by the element $b_{k-(L-1)/2}$ [5]. Otherwise at the higher data rate we will obtain no pseudorandom sequence. Calculating the power density spectrum of the output sequence by Fourier transforming the autocorrelation function, we obtain [8]

$$S(f) = \frac{\frac{L}{2}+1}{4 \cdot \left(\frac{L}{2}\right)^2} \sum_{\mu=-\infty}^{\infty} \mathrm{Si}^2\left(\frac{\mu \cdot \mathrm{p}}{\mathrm{L}}\right) \cos^2\left(\frac{(2\gamma+1) \cdot \mu \cdot \mathrm{p}}{\mathrm{L}}\right) \tag{1}$$

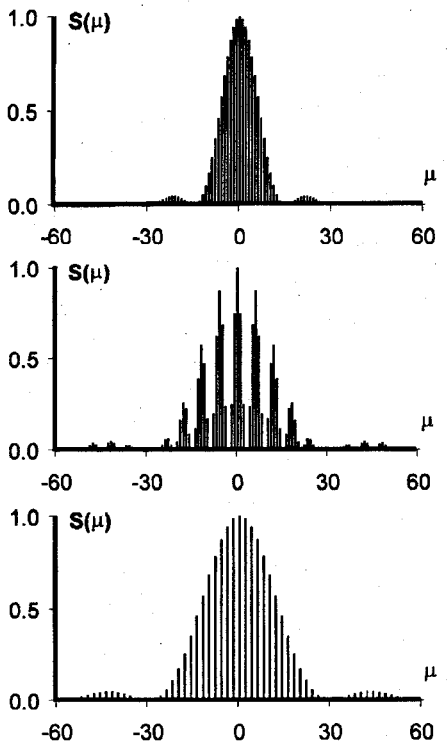

Fig. 2. Power density spectra (phase shift γ is set to, respectively, 0, 2 and 7 b; $L = 15$).

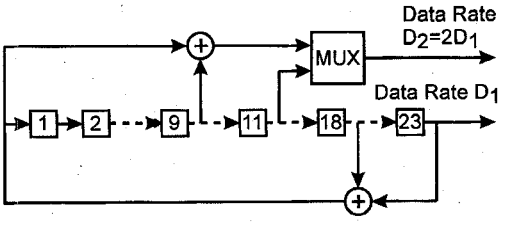

Fig. 3. Operational principle.

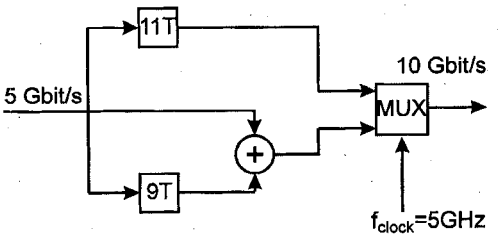

Fig. 4. Block diagram of a multiplexer stage with delay lines.

where L is the length of the sequence. The integer μ is given by

$$\mu = \frac{f}{\Delta f} = f \cdot T_0 \cdot L \tag{2}$$

with Δf, T_0, and γ being the distance of discrete spectral lines, the time duration of one single bit, and the phase shift in bits, respectively. Fig. 2 illustrates that only multiplexing sequences with the correct phase shift produces the desired pseudorandom output sequence. In this example, L is set to 15.

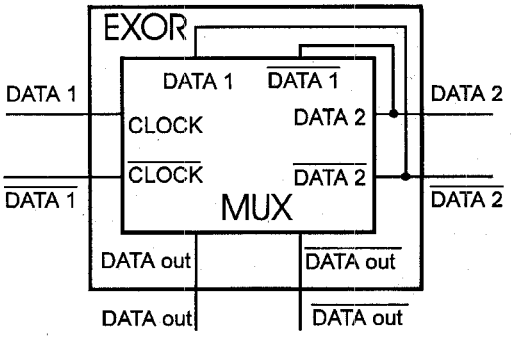

Fig. 5. Implementation of the EXOR-gate using a multiplexer.

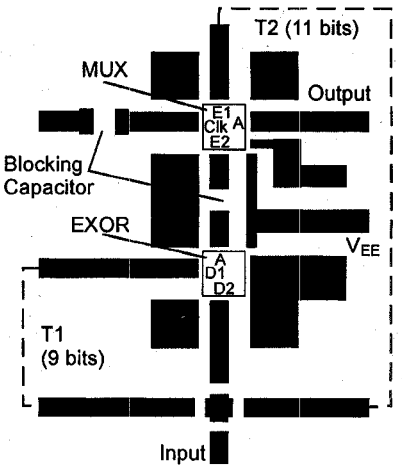

Fig. 6. Layout of the 10 Gb/s structure.

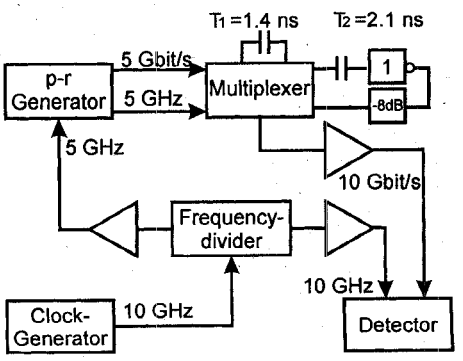

Fig. 7. 10 Gb/s block diagram.

If we have to deal with long sequences, the required phase shift of $(L-1)/2$ bits cannot be implemented directly, e.g., by the use of a delay line. To overcome this problem, we make use of the "cycle-and-add-property" of pseudorandom sequences [6] which is as follows. Modulo 2 adding of two identical but phase-shifted pseudorandom sequences produces the same sequence with a different but well-defined phase. There are several algorithms to calculate the combinations necessary to obtain a special phase of the output sequence [4], [5], [9]–[12]. According to *Eier and Malleck*, the generation of pseudorandom sequences can be described as the quotient of a decoupling polynomial $H(D)$ that determines the phase of the sequence, and a feedback polynomial $A(D)$ that determines

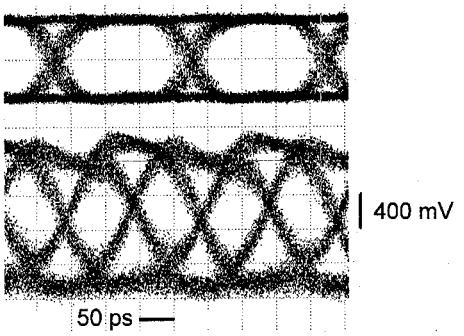

Fig. 8. Eye diagram of the 10 Gb/s output sequence.

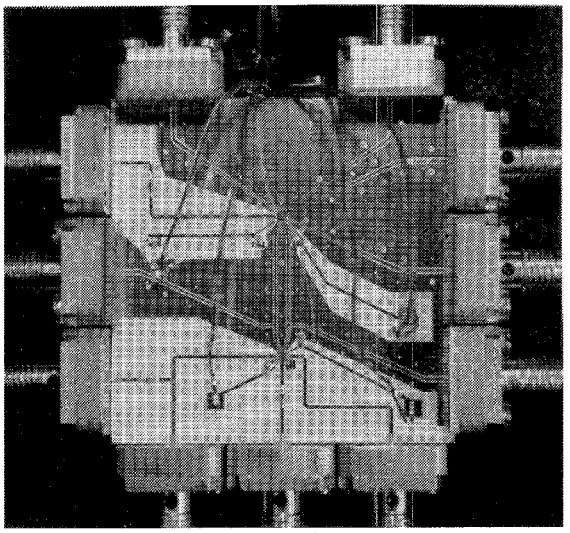

Fig. 9. 20 Gb/s circuit.

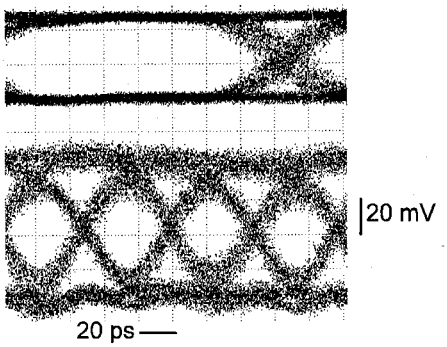

Fig. 10. Eye diagram of a 5 Gb/s input and a 20 Gb/s output sequence.

the characteristic of the sequence itself. This quotient can also be written as the infinite series

$$\frac{H(D)}{A(D)} = m_0 D^0 \oplus m_1 D^1 \oplus \cdots = \sum_{r=0}^{\infty} m_r D^r. \tag{3}$$

Separating this series in even and odd clock cycles as is described above, we obtain

$$\frac{H(D)}{A(D)} = \left(\sum_{r'=0}^{\infty} m_{2r'} D^{2r'}\right) + D \cdot \left(\sum_{r'=0}^{\infty} m_{2r'+1} D^{2r'}\right) \tag{4}$$

using two series composed of D^2 terms and thus yielding at a lower data rate. Since these series must be identical with the

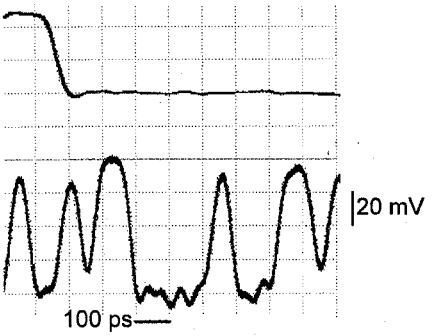

Fig. 11. Portion of a 5 Gb/s input and a 20 Gb/s output sequence.

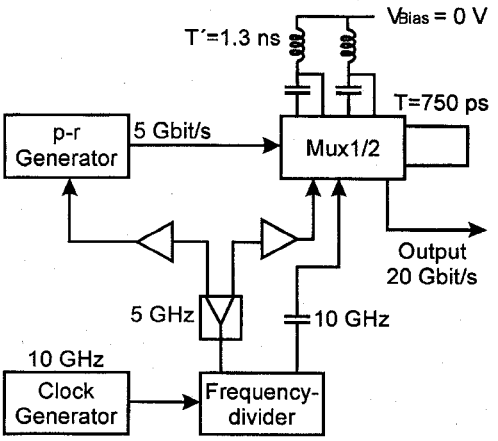

Fig. 12. Block diagram of the structure producing the 20 Gb/s sequence.

original one [5] (not considering data rate and phase shift), they can be described using the same feedback polynomial $A(D)$. Therefore, we can substitute

$$\sum_{r=0}^{\infty} m_{2r} D^{2r} = \frac{G(D^2)}{A(D^2)} \tag{5}$$

$$\sum_{r=0}^{\infty} m_{2r+1} D^{2r} = \frac{U(D^2)}{A(D^2)}. \tag{6}$$

On the other hand, inverting this procedure by combining two slower ones, the generation of a fast sequence is described by

$$\frac{H(D)}{A(D)} = \frac{G(D^2)}{A(D^2)} + D \cdot \frac{U(D^2)}{A(D^2)}. \tag{7}$$

For these kinds of polynomials, we have [6]

$$(P(D))^2 = P(D^2) \tag{8}$$

yielding the slower sequence

$$G(D^2) = (H(D) \cdot A(D))_{\text{even}}, \tag{9}$$

$$D \cdot U(D^2) = (H(D) \cdot A(D))_{\text{odd}}. \tag{10}$$

Since we do not have to consider the phase of the generated sequence, we define

$$H(D) \equiv 1. \tag{11}$$

Applying this procedure to the CCITT standard sequence given in [7], we obtain

$$G(D) = 1 + D^9, \tag{12}$$

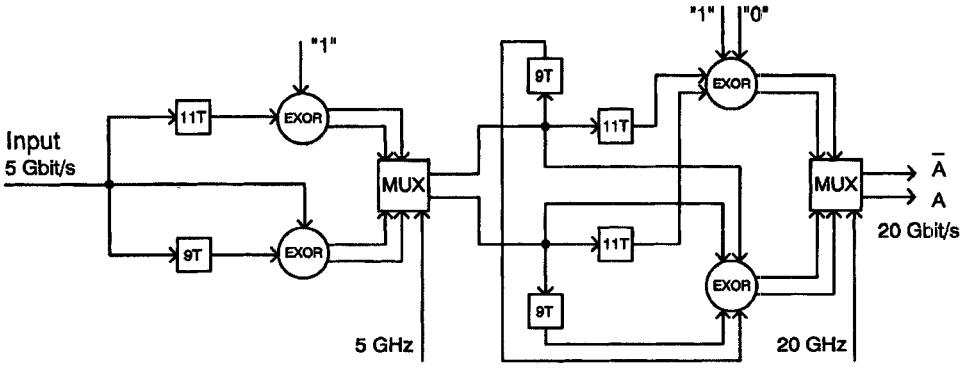

Fig. 13. Block diagram to generate a 20 Gb/s pseudorandom sequence.

$$U(D) = D^{11} \tag{13}$$

represented by the block diagram shown in Fig. 3. Since we do not have access to the internal shift register stages, the three different sequences are provided by delayed versions of the output sequence (Fig. 4)

III. Circuit Principle

For the realization of the 20 Gb/s pseudorandom multiplier, circuits were used, which were fabricated in a silicon bipolar laboratory technology [13]. The circuits are based on E^2CL-logic in differential operation. An excellent performance is achieved because all inputs and outputs are terminated with 50 Ω on-chip resistors providing very good matching and reducing the time-jitter. Furthermore, the circuits work with only a single supply voltage of −5 V consuming 280 mW of power.

The EXOR-gate was built using a multiplexer-chip, where the clock is used as the first input of the EXOR and the combination of data 2 and the inverted data 1 is used as the second input (Fig. 5).

IV. Experimental Results

A circuit providing a 10 Gb/s pseudorandom sequence was realized in microstrip technology on a standard alumina substrate (Fig. 6). The NRZ input signal is split into three paths 1, 2, and 3, using a resistive and therefore broadband power divider. The signal of path 1 is fed to an EXOR gate circuit whose second input is the NRZ input signal delayed by 9 b. The output signal of the EXOR chip is one of the input signals of the multiplexer. The second multiplexer input signal is given by the NRZ input signal delayed by 11 b. The delay times are provided by external coaxial lines and consider the different lengths of the signal paths on the substrate. In order to achieve equal power levels, an 8 dB attenuator was inserted into the line connecting the power divider and the multiplexer chip. Since the EXOR-chip produces an inverted replica of the delayed sequence, an additional inverter was provided to correct the second input signal of the multiplexer. The use of external delay lines additionaly provides a feasible way to overcome crossings in the signal paths, that are necessary due to the given contact pads of the chips. During the experimental stage of the work, the delay times are provided by variable delay lines. Once tuned correctly, they are then replaced by appropriate coaxial lines. Both the 5 Gb/s input and the multiplexer clock-signal are fed via blocking capacitors. At the four edges the chips are contacted to ground pads which are connected to the substrate ground by several via holes. The chips, which here are operated single-endedly, are contacted by bond wires. To keep these as short as possible in order to avoid matching problems, the chips are mounted into holes in the alumina substrate.

To synchronize the pseudorandom sequence generator, the bit error detector and the multiplexer, a frequency divider stage is used to provide appropriate clock signals [14]. Fig. 7 gives the complete block diagram including the frequency divider and delay lines as well as the generator and the detector. Fig. 8 shows the eye diagram of the 10 Gb/s output sequence.

A further structure using two multiplexers generates a 20 Gb/s sequence (Fig. 9). In this case the input signal is split into two paths 1 and 2, which are fed to the multiplexer chip. One of the two signals is delayed by 750 ps while passing an external coaxial line. Due to the high data rate, the second multiplexer stage is operated differentially, thus improving the symmetry of the output sequence. The two output signals OUT and $\overline{\text{OUT}}$ of the first multiplexer stage are treated the same way as the first input signal, i.e., they are split up and fed to the inputs data1, data2, and $\overline{\text{data1}}$, $\overline{\text{data2}}$, respectively. A symmetric output signal requires an exact symmetry of the two dalay lines, which produce a time shift of 1.3 ns. The RF interconnection lines were fabricated in coplanar waveguide technology. This enables tapering the waveguides toward the chips while maintaining the characteristic impedance of 50 Ω. Therefore matching not only of the impedance but also of the field profile is achieved. Another advantage of coplanar waveguide technology compared to microstrip lines is that a better performance can be achieved with respect to dispersive effects [15], [16], which can not be neglected at these data rates and transmission line lengths. To synchronize the single stages, all clock signals are provided by a frequency divider stage. Figs. 10 and 11 show respectively the eye diagram and portions of the 5 Gb/s input and of the 20 Gb/s output signal. Fig. 12 gives the block diagram of the circuitry producing the 20 Gb/s sequence.

Fig. 13 gives the block diagram of a circuit generating a 20 Gb/s pseudorandom sequence. Additional EXOR-chips in both

stages enable differential and therefore symmetrical operation of all important chips. Also the use of additional inverters is then unnecessary. Connections are made using coplanar waveguides that are tapered to contact both the chips and the plugs. Delay times are provided using external coaxial lines.

V. Conclusion

We succesfully used a multiplex-technique to multiply the data rate of a 5 Gb/s pseudorandom sequence to 10 Gb/s. A 20 Gb/s circuitry permits the derivation of a block diagram of a circuit which enables the generation of a 20 Gb/s pseudorandom sequence using the same operational principle, operating all chips differentially, and employing coplanar waveguide technology.

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References

[1] F. Matera and M. Settembre, "Comparison of the performance of optically amplified transmission systems," *J. Lightwave Technol.,* vol. 14, pp. 1–12, Jan. 1996.

[2] K. H. Kim, H. K. Lee, S. Y. Park, and E.-H. Lee, "Calculation of dispersion and nonlinear effect limited maximum TDM and FDM bit rates of transform-limited pulses in single-mode optical fibers," *J. Lightwave Technol.,* vol. 13, pp. 1997–1604, Aug. 1995.

[3] L. Treitinger, A. Felder, R. Köpl, T. F. Meister, S. Pick, J. Popp, R. Schreiter, P. Weger, J. Wieland, and H.-M. Rein, "Silicon technologies and integrated circuits for multi Gbit/s light-wave communication at 10-100 Gb/s," in *Proc. 19th European Conf. Optic. Commun.,* pp. 76–79, 1993.

[4] R. Eier and H. Malleck, "Anwendung von Multiplextechniken bei der Erzeugung von schnellen Pseudozufallsfolgen," *Nachrichtentechnische Zeitschrift,* pp. 227–231, 1975 (in German).

[5] K. H. Möhrmann, "Erzeugung von Quasi-Zufallsfolgen hoher Takfrequenz durch Multiplexen," *Siemens Forschungs- und Entwicklungsberichte,* pp. 218–224, 1974 (in German).

[6] S. W. Golomb, *Shift Register Sequences.* San Francisco, CA: Holden-Day, 1967.

[7] "Error performance measuring equipment operating at the primary rate and above," in *CCITT Series O Recommendation, O.151,* Geneva, Switzerland: Int. Telecommun. Union, 1992. Rev. 1.

[8] R. Eier and H. Malleck, "Charakterisierung und Erzeugung von verwürfelten m-Folgen," *Archiv für Elektronik und Übertragungstecknik,* pp. 319–27, 1976 (in German).

[9] W. D. T. Davies, "Generation and properties of maximum-length sequences," *Control,* pp. 302–304, 1966.

[10] A. C. Davies, "Delayed versions of maximal-length linear binary sequences," *Electron. Lett.,* vol. 1, pp. 61–62, May 1965.

[11] S. H. Tsao, "Generation of delayed replicas of maximal-length linear binary sequences," *Proc. IEE,* vol. 111, pp. 1803–1806, Nov. 1964.

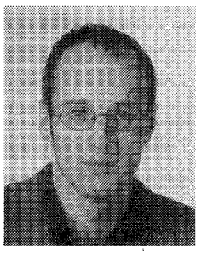
[12] A. G. Gardiner, "Logic p.r.b.s. delay calculator and delayed version generator with automatic delay-changing facility," *Electron. Lett.,* vol. 1, pp. 123–124, July 1965.

[13] A. Felder, R. Stengel, J. Hauenschild, H.-M. Rein, and T. F. Meister, "25 Gbit/s decision circuit, 34 Gbit/s multiplexer, and 40 Gbit/s demultiplexer in selective epitaxial si bipolar technology," *Electron. Lett.,* vol. 29, pp. 525–526, 1993.

[14] A. Felder, P. Weger, E. Bertagoulli, K. Ehinger, J. Hauenschild, and H.-M. Rein, "A si bipolar 23 Gbit/s multiplexer and a 15 GHz 2:1 static frequency divider," in *Proc. 1991 IEEE Bipolar Circuits Technol. Meeting,* 1991, pp. 31–34.

[15] M. Riaziat, R. Majidi-Ahi, and I. Feng, "Propagation modes and dispersion characteristics of coplanar waveguides," *IEEE Trans. Microwave Theory and Techniques,* pp. 245–251, Mar. 1990.

[16] Y. S. Shih and T. Itoh, "Analysis of conductor-backed coplanar waveguide," *Electron. Lett.,* vol. 18, pp. 538–540, June 1982.



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